REMARKS

In the final Office Action, claims 1-4, 6-31, and 33-58 were rejected. Claims 1-4, 6-31, and 33-58 remain pending. Applicants request reconsideration of the pending claims.

I. Claim Rejections – 35 USC 102

Claims 1-2, 12-15, 26-29, 37, 39-42, and 56-58 stand rejected under 35 USC 102 as being anticipated by US Patent No. 5,831,446 (the So reference).

Applicants have asserted that the So reference fails to disclose or suggest that the 30 chains disclosed in the So reference are arranged as a padgroup so that they can be tested **together** (i.e., tested at approximately the same time) when they are connected electrically in parallel. In the final Office Action, the Examiner responded by simply stating that the So reference teaches "the test pads tested in parallel."

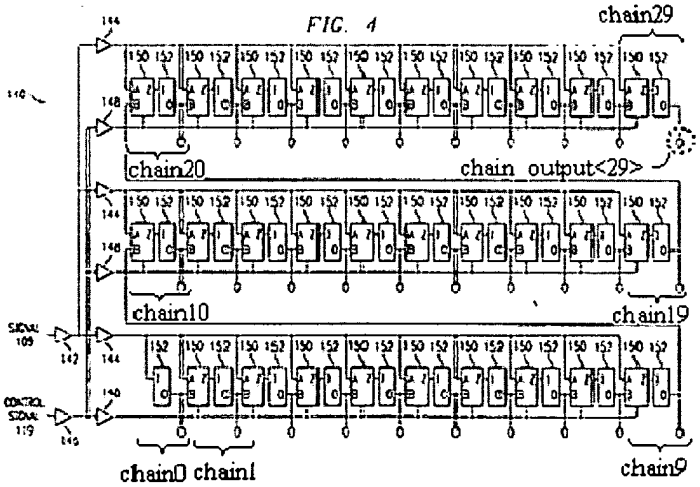
As an initial matter, Applicants not that the term "parallel" could have two possible meanings: one meaning is electrical (i.e., two chains are connected electrically in parallel such that the output of one is not the input of another); and another meaning is temporal (i.e., two chains are tested at approximately the same time). These two meanings are not synonymous and should not be conflated. In other words, testing two chains connected electrically in parallel does not necessarily require that they be tested at approximately the same time. For example, assume that two chains are connected electrically in parallel (i.e., the output of one chain is not the input of another chain). One of the two chains can be tested at one time, and then the other chain can be tested at a later time. In this example, the two chains are tested in parallel because the two chains are connected electrically in parallel (i.e., the output of one chain is not the input of another chain) even though they were tested at different times.

In the present application, independent claims 1, 28, and 58 explicitly recite that the test structures in a padgroup are electrically tested "**together in parallel**." Thus, the term "**together**" requires that the test stuctures in the padgroup are tested at approximately the same time, while the

term "**parallel**" requires the test structures are connected electrically in parallel when they are tested at approximately the same time.

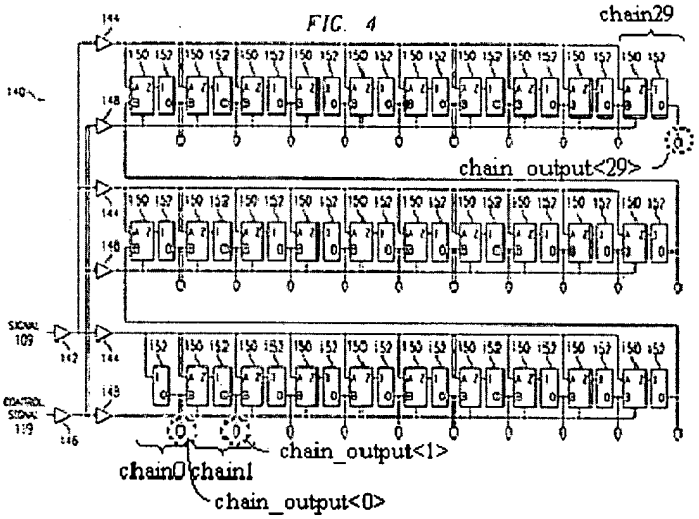
In contrast, Applicants assert that the So reference only uses the term "parallel" consistent with the electrical meaning (i.e., that the chains are connected electrically in parallel). In particular, FIG. 4 of Reference 1 depicts 30 chains, which are tested in series and in parallel.

When tested in series, the output of one chain is connected to the input of a subsequent chain, which is consistent with the electrical meaning of the term "series." For example, as shown in the annotated copy of FIG. 4 below, the output of chain0 is connected to the input of chain1 through input "B" of multiplexing element 150 of chain1. Similarly, the output of chain9 (last chain in first row) is connected to the input of chain10 (first chain in second row); and the output of chain19 (last chain in second row) is connected to the input of chain20 (first chain in third row). Because the 30 chains are connected in series, the entire chain of 30 chains is tested by reading from the output of the last chain (i.e., chain_output<29> of chain 29). Thus, if there is any fault in any one or more of the chains, then the fault can be detected by reading chain_output<29>.



When tested in parallel, each input of each chain is provided by signal 109 through input "A" of multiplexing element 150 rather than receiving the output of a previous chain through input "B" of multiplexing element 150, which is consistent with the electrical meaning of the term "parallel." The output of each chain is tested using an output pad for each output signal. For

example, as shown in the annotated copy of FIG. 4 below, the output of chain0 is tested using an output pad for chain_output<0>; and the output of chain1 is tested using a separate output pad for chain_output<1>. Thus, each chain is tested by reading the individual output for each of the chain.



The So reference does not disclose arranging the output pads of the chains into pad groups to allow for multiple outputs of multiple chains to be read at approximately the same time. Instead, each output pad is depicted separated from one another. For example, as shown above in the annotated version of FIG. 4, the output pad for chain0 labeled with output_signal<0> is separated from the output pad of chain1 labeled with output_signal<1>. No group of output pads are shown as being arranged in a pad group that would allow for the output pads to be tested together (at approximately the same time).

Moreover, Applicants assert that the So reference teaches away from testing the chains at approximately the same time when they are connected electrically in parallel because testing the chains at approximately the same time makes the serial mode redundant. In particular, in the So reference, the serial mode is used to quickly test all 30 chains together at the same time using one output (chain_output<29>). If the chain of 30 chains passes the serial mode test, then all 30 of the chains in the chain are good because they are connected in series. In this case, there is no need to perform the parallel mode test. If the chain of 30 chains fails the serial mode test, then one or more

of the 30 chains is bad, but it is not known from the serial mode test which one(s) because they are connected in series. In this case, the parallel mode test is needed to test each chain one at a time to pinpoint the bad chain(s). Thus, the purpose of the serial test mode, which allows all 30 chains to be tested together at the same time, is to avoid having to test each chain one at a time during the parallel test mode, which is time consuming. If all 30 chains could be tested together at the same time during the parallel test mode, then the serial test mode would not be necessary.

Thus, Applicants assert that claims 1, 28, and 58 are allowable over the So reference. Applicants also assert that claims 2, 12-15, 26, 27, 29, 37, 39-42, 56, and 57, which variously depend on claims 1 and 28, are allowable for at least the reason that they depend from allowable independent claims.

II. Claim Rejections – 35 USC 103

Claims 3, 4, 30, 31, and 43-45 were rejected under 35 USC 103(a) over the So reference in view of US Patent No. 6,291,254 (the Chou reference). These claims variously depend from independent claims 1 and 28, which are allowable over the So reference for at least the reasons set forth above. Thus, Applicants assert that claims 3, 4, 30, 31, and 43-45 are allowable for at least the reason that they depend from allowable independent claims.

Claims 6-11, 18-20, 33-38, and 48-50 were rejected under 35 USC 103(a) over the So reference in view of US Patent No. 5,666,049 (the Yamada reference). These claims variously depend from independent claims 1 and 28, which are allowable over the So reference for at least the reasons set forth above. Thus, Applicants assert that claims 6-11, 18-20, 33-38, and 48-50 are allowable for at least the reason that they depend from allowable independent claims.

Claims 16, 17, 46, and 47 were rejected under 35 USC 103(a) over the So reference in view of UPAP 2004/0094762 (the Hess reference). These claims variously depend from independent claims 1 and 28, which are allowable over the So reference for at least the reasons set forth above. Thus, Applicants assert that claims 16, 17, 46, and 47 are allowable for at least the reason that they depend from allowable independent claims.

Claims 21-25 and 51-55 were rejected under 35 USC 102(a) over the So reference in view of the Yamada reference and the Kim reference. These claims variously depend from independent claims 1 and 28, which are allowable over the So reference for at least the reasons set forth above. Thus, Applicants assert that claims 21-25 and 51-55 are allowable for at least the reason that they depend from allowable independent claims.

III. Conclusion

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 524322000300. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: March 25, 2008

Respectfully submitted,

By /Peter J. Yim/

Peter J. Yim
Registration No.: 44,417
MORRISON & FOERSTER LLP
425 Market Street
San Francisco, California 94105-2482
Telephone: (415) 268-6373
Facsimile: (415) 268-7522